REMARKS

The Office Action mailed April 6, 2006, has been received and reviewed. Claims 1-14 and 25-39 are currently pending in the application. Claims 1-14 and 25-39 each presently stand rejected. Applicants respectfully request reconsideration of the application herein.

35 U.S.C. § 102 Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 6,680,241 to Okamoto, *et al.*

Claims 1, 2, 4-14, 25, and 29-34 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Okamoto, *et al.*, U.S. Patent No. 6,680,241 (hereinafter "Okamoto"). Applicants respectfully traverse this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

With respect to inherency, "the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic." *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); M.P.E.P § 2112(IV)(emphasis in original). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily in the thing described in the reference and that it would be so recognized by persons of ordinary skill...The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999); M.P.E.P § 2112(IV). "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990)(emphasis in original); M.P.E.P § 2112(IV).

Independent claim 1 recites a method for supporting wafers for singulation and pick-and-place. The method comprises providing a semiconductor wafer; mounting an

adhesive-coated tape to a surface of the semiconductor wafer; gripping the semiconductor wafer *along at least a portion of a periphery thereof*; singulating individual components from the semiconductor wafer, *leaving a ring of material comprising at least in part a material of the semiconductor wafer along the periphery thereof*; and removing at least some individual components from the adhesive-coated tape.

Pertaining to claim 1, Okamoto discloses a method of improving the flexural strength of a chip by reducing the chipping and cracking of the chip that occurs during the processing of the chip. Col. 1, lines 35-39. In the method, a wafer sheet 2 is bonded to the front surface 1a of a 200 mm silicon wafer 1. Col. 2, lines 22-26; FIG. 1A. A grindstone 3 polishes the back surface 1b of the wafer 1. Col. 2, lines 26-27; FIG. 1A. Subsequently, a wafer sheet 5 is bonded to the back surface 1b of the wafer 1. Col. 2, lines 37-38; FIG. 1C. A *stainless steel* frame 6 of a ring shape "physically supports the wafer sheet 5." Col. 2, lines 40-43; FIG. 1C. The wafer sheet 2 is removed from the wafer 1 and the wafer 1 is diced along scribe lines on the front surface 1a. Col. 2, lines 43-48; FIGS. 1C-1D. A wafer sheet 10 with a frame 11, apparently a stainless steel frame as described earlier with respect to frame 6, is applied to the front surface 1a and the wafer sheet 5 is removed. Col. 2, lines 48-51; FIG. 1D.

Okamoto, however, does not expressly or inherently describe every element of independent claim 1. Among others, Okamoto does not disclose gripping the semiconductor wafer in any manner. During the entire dicing process, Okamoto provides no detail as to how the wafer and the associated wafer sheets 5, 10 and their respective frames 6, 11 are supported. Indeed, the nearest description that Okamoto provides as to how the wafer is supported is that the wafer sheet 10 with "ring-shaped frame 11 at the *outer periphery of the sheet* 10" is "placed" on the upper surface of a stage 54 in a vacuum chamber. Col. 5, lines 54-63; FIG. 5. With respect to the wafer sheets 2, 5,10, 20, 30, and 35, they are "bonded" (Col. 2, lines 22, 43, 49, 52; Col. 3, line 19; Col. 4, lines 46, 56; Col. 5, lines 27, 60; FIGS. 1-5) or "adhered" (Col. 3, line 25; FIG. 1G) to the wafer. Thus, Okamoto does not disclose a method of gripping a semiconductor wafer along a portion of the wafer's periphery.

Additionally, Okamoto does not disclose a method that includes singulating components from a wafer and leaving a ring of material that is *comprised in part of the material from the*

wafer. It is respectfully noted that the drawings disclose a wafer 1 bonded to a wafer sheet 5 that is supported by a stainless steel ring 6. Col. 2, lines 37-44; FIG. 1B. The wafer sheet, however, is not a part of the material of the semiconductor material. Rather, it is quite a distinct and separate item as Okamoto repeatedly states throughout the specification, a point, it is respectfully noted, that the examiner apparently recognizes implicitly when describing the wafer sheet as "adhesive-coated tape." *See, e.g.*, Office Action of April 6, 2006, pg. 3.

Thus, in view of the foregoing arguments, Okamoto does not either expressly or inherently disclose each and every element of independent claim 1. Therefore, the withdrawal of the 35 U.S.C. § 102(e) rejection of independent claim 1 is respectfully requested.

Further, the withdrawal of the 35 U.S.C. § 102(e) rejections of claims 2 and 4-14 is respectfully requested as each claim depends either directly or indirectly from allowable independent claim 1, among other reasons.

Claim 2 is additionally allowable because Okamoto does not disclose expressly or inherently gripping the semiconductor wafer by the ring of material (which, as now recited in claim 1, includes a material of the semiconductor wafer) along at least a portion of the periphery thereof during the removing of the at least some individual components.

Claim 4 is additionally allowable because Okamoto does not disclose expressly or inherently forming at least a portion of the ring of material from a polymer material disposed about and contiguous with a periphery of the semiconductor wafer and of thickness at least as great as a thickness of the semiconductor wafer. As discussed above, Okamoto does not disclose a ring of material formed from a wafer. Nor does Okamoto expressly or inherently disclose a ring of material formed from a polymer. Rather, Okamoto discloses a thin, reinforcing film 15 formed in a layer by spin coating. Col. 2, lines 65-67; Col. 3, lines 1-17; FIG. 1E. Additionally, as Okamoto notes, the polyimide film 15 is 10 μm or thinner as compared to post-backgrinding wafer thickness of 100 μm. Col. 4, lines 10-11, 17-20.

Claim 5 is additionally allowable because Okamoto does not disclose expressly or inherently forming the ring in part from the material of the semiconductor wafer and in part from a polymer disposed about and contiguous with a periphery of the semiconductor wafer and of thickness at least as great as a thickness of the semiconductor wafer, as discussed vis-à-vis

claim 4.

Claim 6 is additionally allowable because Okamoto does not disclose expressly or inherently forming the ring of material disposed about a periphery from a polymer material by one of spin-coating, stereolithography or molding. Okamoto disclose spin coating within the context of forming a uniform polyimide reinforcing film, not a ring of material, as discussed above vis-à-vis claim 4.

Claim 8 is additionally allowable because Okamoto does not disclose expressly or inherently a method that includes singulating the semiconductor wafer from a backside of the wafer. Rather, Okamoto discloses dicing the wafer 1 along scribe lines formed on the front surface 1a of the wafer 1. Col. 2, lines 46-47; FIG. 1D.

Claim 12 is additionally allowable because Okamoto does not disclose expressly or inherently a method that includes exposing a UV-sensitive adhesive prior to removing the at least some individual components while leaving a portion on the adhesive-coated tape extending over the ring of material unexposed. Rather, Okamoto describes applying ultraviolet rays to apparently the entire wafer sheet 10 so that the wafer sheet 10 may be removed from the chips 1c. Col. 3, lines 21-23; FIG. 1F.

Independent claim 25 recites in part a method for processing a semiconductor wafer that includes singulating individual components from the semiconductor wafer...*without using a film frame while the adhesive-coated tape is mounted to the surface thereof.*

The disclosure of Okamoto, however, is limited to using a stainless steel frame 6, 11, 21, 31, and 36. *See* FIGS. 1-5. As discussed with respect to claim 1, Okamoto provides no indication of how the wafer sheets are supported beyond the frames and being set on the stage 54. The only indication that Okamoto provides that a film frame is unnecessary is during the formation of *grooves* 32 in the wafer 1. Col. 4, lines 51-55. In that instance, the silicon wafer 1 may have the grooves formed by "directly sucking it to a dicing stage, without bonding the wafer sheet 30. A wafer sheet without a frame may be used." Col. 4, lines 52-54; FIG. 3A. It is critical, however, that Okamoto immediately discloses using a wafer sheet 35 *with a frame* 36 for the subsequent grinding process. Col. 4, lines 55-57; FIG. 3B. The wafer is ground until the groove 32 is exposed, thus singulating the chips. Col. 5, lines 57-59; FIG. 3B.

Therefore, Okamoto uses a frame 36 to support the wafer sheet 35 during the grinding process that singulates the chips 1c.

Therefore, in view of the foregoing, the withdrawal of the 35 U.S.C. § 102(e) rejection of independent claim 25 is respectfully requested.

Independent claim 29 recites a method of processing a semiconductor wafer that includes gripping a semiconductor wafer along at least a portion of the wafer's periphery and singulating the semiconductor wafer into individual components while leaving an uncut peripheral ring of material thereabout.

Okamoto, however, does not disclose expressly or inherently each and every element of independent claim 29. As with independent claim 1 discussed above, Okamoto does not disclose expressly or inherently gripping the semiconductor wafer in any manner, among others. Nor does Okamoto disclose expressly or inherently a method of singulating individual components while leaving an uncut peripheral ring of material thereabout, also as discussed above vis-à-vis independent claim 1.

Therefore, in view of the foregoing, the withdrawal of the 35 U.S.C. § 102(e) rejection of independent claim 29 is respectfully requested.

The withdrawal of the 35 U.S.C. § 102(e) rejection of claims 30-34 is respectfully requested as each depends either directly or indirectly upon allowable independent claim 29, among other reasons.

Claim 31 is additionally allowable because Okamoto does not disclose gripping the uncut peripheral ring of material comprising at least in part a material of the semiconductor wafer while removing the at least some singulated individual components. As discussed above, Okamoto discloses solely singulating and removing die components through the use of a wafer sheet frame. Okamoto never discloses gripping the semiconductor wafer or any ring of material.

Claim 32 is additionally allowable because Okamoto does not disclose defining an uncut peripheral ring of material from semiconductor material.

Claim 33 is additionally allowable because Okamoto does not disclose defining an uncut peripheral ring of material at least in part from a polymer disposed about and contiguous with the semiconductor wafer, as discussed above with respect to claim 4.

Claim 34 is additionally allowable because Okamoto does not disclose an uncut peripheral ring of material at least in part from semiconductor material and in part from a polymer disposed about and contiguous with the periphery of the semiconductor wafer, as discussed above with respect to claim 5.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 6,680,241 to Okamoto, *et al.*, in view of U.S. Patent Application Publication 2003/0003688 to Tandy, *et al.*

Claim 3 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Okamoto in view of Tandy, *et al.*, U.S. Patent Application Publication 2003/0003688 (hereinafter "Tandy"). Applicants respectfully traverse this rejection, as hereinafter set forth.

> M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:
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> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claim 3 is improper because the non-obviousness of independent claim 1 precludes a rejection of claim 3 which depend therefrom; a dependent claim is obvious only if the independent claim from which it depends is obvious. *See* In re Fine, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988), *see also* MPEP § 2143.03. Therefore, the withdrawal of the 35 U.S.C. § 103(a) obviousness rejection of dependent claim 3, which depends upon non-obvious independent claim 1 is respectfully requested.

Further, neither Okamoto nor Tandy provides a suggestion or motivation to combine the references. Okamoto, as discussed above, relates to methods of using a wafer sheets and frames during a spin coating and singulating process. Tandy, conversely, relates to methods of marking semiconductor wafers and devices. The only apparent motivation to combine the references is

improper hindsight. Therefore, the withdrawal of the 35 U.S.C. § 103(a) obviousness rejection of dependent claim 3, is respectfully requested.

Obviousness Rejection Based on U.S. Patent No. 6,680,241 to Okamoto, *et al.*, in view of U.S. Patent No. 6,551,906 to Oka

Claims 26-28 and 35-39 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Okamoto in view of Oka, U.S. Patent No. 6,551,906 (hereinafter "Oka"). Applicants respectfully traverse this rejection, as hereinafter set forth.

The 35 U.S.C. § 103(a) obviousness rejections of claims 26-28 are improper because the non-obviousness of independent claim 25 precludes a rejection of claims 26-28 which depend therefrom; a dependent claim is obvious only if the independent claim from which it depends is obvious. *See* In re Fine, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988), *see also* MPEP § 2143.03. Therefore, the withdrawal of the 35 U.S.C. § 103(a) obviousness rejection of dependent claims 26-28, which depends upon non-obvious independent claim 25, is respectfully requested.

Claim 26 is additionally allowable because neither Okamoto nor Oka teaches or suggests a method that includes handling a 300 mm semiconductor wafer using equipment sized to handle 200 mm semiconductor wafers. Rather, Oka teaches, in figures 1A-7H and corresponding text, a method of grinding a semiconductor wafer to desired *thickness* prior to singulation.

Claim 27 is additionally allowable because neither Okamoto nor Oka teaches or suggests a method that includes singulating the 300 mm semiconductor wafer using a 200 mm semiconductor wafer saw chuck.

Claim 28 is additionally allowable because neither Okamoto nor Oka teaches or suggests a method that includes holding the 300 mm semiconductor wafer in a 200 mm semiconductor wafer pick-and-place machine chuck while removing the at least some singulated individual components.

The 35 U.S.C. § 103(a) obviousness rejections of claims 35-37 are improper because the non-obviousness of independent claim 29 precludes a rejection of claims 35-37 which depend therefrom. *See* In re Fine, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988), *see also* MPEP § 2143.03. Therefore, the withdrawal of the 35 U.S.C. § 103(a) obviousness rejection of dependent claims

35-37, which depends upon non-obvious independent claim 29, is respectfully requested.

Claim 35 is additionally allowable because neither Okamoto nor Oka teaches or suggests a method that includes handling a 300 mm semiconductor wafer using equipment sized to handle 200 mm semiconductor wafers.

Claim 36 is additionally allowable because neither Okamoto nor Oka teaches or suggests a method that includes singulating the 300 mm semiconductor wafer using a 200 mm semiconductor wafer saw chuck.

Claim 37 is additionally allowable because neither Okamoto nor Oka teaches or suggests a method that includes holding the 300 mm semiconductor wafer in a 200 mm semiconductor wafer pick-and-place machine chuck while removing the at least some singulated individual components.

Independent claim 38 is allowable because neither Okamoto nor Oka teaches or suggests a method that includes handling a 300 mm semiconductor wafer with equipment sized to handle 200 mm semiconductor wafers, as discussed with respect to claims 26 and 28. Therefore, the withdrawal of the 35 U.S.C. § 103(a) rejection of independent claim 38 is respectfully requested.

The withdrawal of the 35 U.S.C. § 103(a) rejection of claim 39 is respectfully requested as it depends directly from allowable independent claim 38, among other reasons. *See* In re Fine, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988), *see also* MPEP § 2143.03.

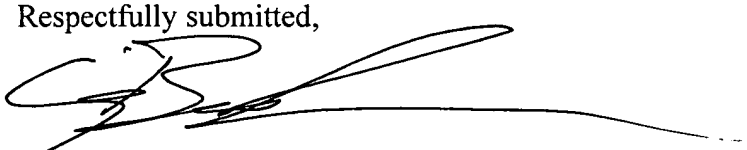
Claim 39 is additionally allowable because neither Okamoto nor Oka teaches or suggests a method that includes processing the 300 mm semiconductor wafer with equipment sized to handle 200 mm semiconductor wafers.

Further, neither Okamoto nor Oka provides a suggestion or motivation to combine the references. Okamoto, as discussed above, relates to methods of using a wafer sheets and frames during a spin coating and singulating process. Oka teaches a method of reducing the thickness of semiconductor wafers, not a method processing 300 mm semiconductor wafers on equipment sized to handle 200 mm wafers. Therefore, there is no motive or suggestion to combine Okamoto with Oka. The only apparent motivation to combine the references is improper hindsight. Therefore, the withdrawal of the 35 U.S.C. § 103(a) obviousness rejection of claims 26-28 and 35-39, is respectfully requested.

CONCLUSION

Claims 1-14 and 25-39 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,



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Date: July 3, 2006

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